This document is a preprint of: D. Swist, S. Friedrich, E. Matus et al., "Power Profiling of a High-Throughput RLL Encoder for THz Communications," in Proceedings of 2026 International Conference on Mobile and Miniaturized Terahertz Systems (ICM2TS 2026), Skukuza, South Africa, Jul 2026.

Power Profiling of a High-Throughput RLL Encoder for THz Communications

Daniel Swist, Simon Friedrich, Emil Matúš, Meik Dörpinghaus, and Gerhard Fettweis
Vodafone Chair Mobile Communications Systems, Technische Universität Dresden, 01062 Dresden, Germany
{daniel.swist, simon.friedrich, emil.matus, meik.doerpinghaus, gerhard.fettweis}@tu-dresden.de

***Abstract*—This paper presents a power-centric profiling of a high-throughput run-length limited (RLL) encoder design for terahertz (THz) communications using zero-crossing modulation (ZXM). Despite the importance of energy efficiency in THz communications, the power efficiency of RLL encoders for ZXM has not been quantified. The evaluation flow runs a power analysis driven by gate-level activity. We compare TSMC 16FFC FinFET CMOS and GlobalFoundries 22FDX FDSOI technologies across multiple threshold-voltage classes and supply-voltage points. We report power consumption and energy-per-bit maps across clock-frequency profiles and various levels of state-merging in the state-machine based RLL encoder design. We identify design configurations that minimize the energy per bit while meeting timing constraints to project feasible system-level implementations beyond 100 Gbps achieving up to 7.2 fJ/bit efficiency. The results provide concrete guidance for selecting operating points for energy-efficient RLL encoder implementations in THz transmitters.**

I. Introduction

High-speed wireless links in the terahertz (THz) range are pushing the digital front-end of transmitters to operate at extreme symbol rates under tight energy budgets. Zero-crossing modulation (ZXM) transceivers are a promising solution for mitigating the energy bottleneck of high-speed analog-to-digital converters (ADC) required for the very high signal bandwidths at THz [1]. This is achieved by using energy-efficient 1-bit quantizers with temporal oversampling [2], [3]. The run-length limited (RLL) encoder is a crucial component of a ZXM system that governs the achievable throughput. While recent work has demonstrated implementation techniques to reach very high throughputs with a parameterizable encoder [4], the power feasibility of such designs across technology nodes, threshold-voltage options, and operating voltages remains insufficiently quantified.

This paper addresses that gap with a power-centric study of a high-throughput RLL encoder design. Especially when high-throughput systems in the range of 100 Gbps [5] to 1 Tbps [6] are considered, power consumption becomes a critical metric. Hence accurate power estimation is essential. We evaluate the power consumption using a unified flow from register-transfer level (RTL) simulation to logic synthesis, gate-level simulation (GLS), and power analysis driven by activity captured at the gate level. In this regard, we compare two mainstream CMOS technologies, TSMC 16FFC FinFET CMOS and GlobalFoundries 22FDX FDSOI, each at several threshold-voltage classes and supply voltages, focusing on operating points at a typical corner of $25\,^{\circ}\mathrm{C}$. We explore a large design space of different clock frequencies and different levels of state merging in the finite-state machine (FSM) based RLL encoder design [2]. The parameter vectors are analyzed jointly to expose architectural trends which are crucial to enhance energy efficiency. A system-level analysis is performed, and several configurations and operating points are identified that minimize the energy-per-bit metric while meeting timing requirements. The system-level analysis indicates feasibility to reach throughputs beyond 100 Gbps.

First, Section II provides the system context, terminology, and the RLL encoder architecture. Section III details the methodology and experimental setup. Section IV presents the power profiling results. Section V reports operating points minimizing energy per bit. Finally, Section VI discusses implications and concludes the paper.

This work is part of the TeraGreen project which received funding from the Smart Networks and Services Joint Undertaking (SNS JU) under the European Union's Horizon Europe research and innovation programme under Grant Agreement No 101139117.

II. System Context

A. ZXM System

One solution to overcome the massive energy bottleneck of the high-speed, high-resolution ADCs required for high-bandwidth terahertz systems is to use energy-efficient 1-bit quantizers. Adopted to this is ZXM, which conveys information in the temporal distances of the zero crossings, where temporal oversampling with respect to the Nyquist rate increases time resolution and thereby enables increasing spectral efficiency [3]. We consider a ZXM system based on [2] which uses RLL-encoded sequences generated in two stages: binary (d, k)-sequence encoding based on FSMs followed by non-return-to-zero-inverse (NRZI) encoding where the parameter d sets the minimum run-length. In [2] RLL codes for different d are given, which enable achieving different spectral efficiencies depending on the oversampling rate $M_{\mathrm{TX}} = d + 1$ of the digital-to-analog converter (DAC) and likewise the ADC. In the digital part of the transmitter, the RLL encoder is a key building block that limits the achievable throughput affecting the entire transceiver chain. In our scope, NRZI mapping to the final line code is handled outside the encoder, so we only consider the core (d, k) FSM encoder. The inherently serial nature of the FSM-based encoder in [2] (see left side of Fig. 1) is challenging for high-throughput implementation [4], especially at multi-hundred-gigabit rates, and

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

This document is a preprint of: D. Swist, S. Friedrich, E. Matus et al., "Power Profiling of a High-Throughput RLL Encoder for THz Communications," in Proceedings of 2026 International Conference on Mobile and Miniaturized Terahertz Systems (ICM2TS 2026), Skukuza, South Africa, Jul 2026.

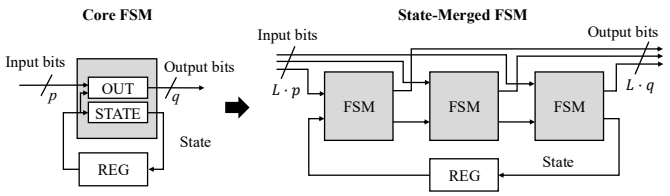

Fig. 1. RLL encoder datapath illustrating state merging for $L = 3$.

consequently poses challenges for power efficiency. Each d corresponds to its own FSM codebook, so each d entails a distinct hardware complexity of the RLL encoder implementation with a different number of states s, and a minimum number of input and output bits per clock cycle, p and q, respectively. Table I summarizes the parameters for the considered RLL encoder where a trend of increasing complexity can be seen with increasing d. Additionally, the code rate r_{RLL} is shown.

B. RLL Encoder RTL Design

The encoder under test is implemented following [4] as a parameterizable RTL design organized as an FSM datapath: state registers feed the next-state and the output logic that maps input bits to constrained output sequences. Additionally, consecutive state transitions can be processed within a single clock cycle. This can be expressed functionally by concatenating individual core FSM components as illustrated in Fig. 1. Although this increases the critical path and logic complexity, throughput gains can be achieved due to the sublinear growth of the critical path compared to the linear increase in number of bits processed per clock cycle [4]. We adopt the term *folding factor* L to describe the number of FSM state transitions processed per clock cycle. Increasing L aggregates more work per cycle and affects power consumption, making it a key parameter in the power analysis. The implementation is a parameterizable Verilog design which is generated based on the following parameters:

- Minimum runlength constraint d of the RLL code
- Folding factor L

Interfaces comprise word-wide input/output buses of size $L \cdot p$ and $L \cdot q$, respectively.

The throughput of the RLL encoder is considered at the input and is defined as $T = p \cdot L \cdot f_{\mathrm{CLK}}$, where $p \cdot L$ is the effective number of input bits processed per clock cycle at folding factor L, and f_{CLK} is the clock frequency of the synthesized netlist. The energy per bit is reported as $E_{\mathrm{b}} = P_{\mathrm{T}}/T$, with the total consumed power P_{T} obtained from power analysis.

TABLE I
RLL ENCODER SYSTEM PARAMETERS PER MINIMUM RUNLENGTH d

d-constraints	1	2	3	4
Number of input bits p	2	1	3	3
Number of output bits q	3	2	7	8
Number of states s	3	4	9	10
RLL code rate $r_{\mathrm{RLL}} = p/q$	2/3	1/2	3/7	3/8

III. METHODS AND SETUP

A. Toolflow

The four-stage analysis flow is shown in Fig. 2:

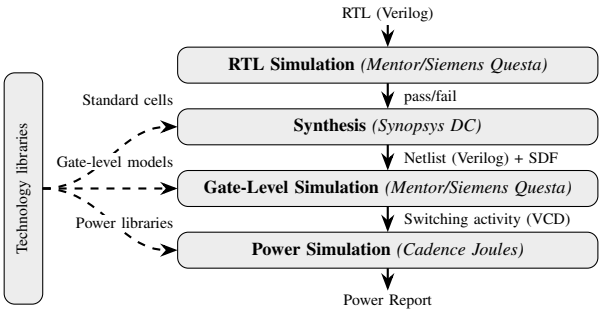

Fig. 2. Top-to-bottom methodology of tool flow.

RTL simulation: The parameterized RTL is simulated within a testbench. The encoder parameters under test are the RLL constraint d and the folding factor L.

Synthesis: The RTL is synthesized for the selected technology libraries at each operating point, producing the gate-level Verilog netlist and design constraints in Standard Delay Format (SDF) as the authoritative output for downstream GLS and power analysis.

Gate-level simulation: The synthesized netlist, with SDF delay annotation, is simulated in the same testbench as used for the RTL simulation using the technology libraries to verify cycle-accurate behavior against the reference and to capture switching activity in a Value Change Dump (VCD) file for power analysis.

Power simulation: The gate-level netlist and activity traces at the intended operating corner are fed to the power simulation to report power consumption and its breakdown into internal, switching, and leakage. Only *timing-clean* points (non-negative slack at the target frequency) are considered in comparisons.

The entire flow is automated via scripts to sweep the design parameters, operating points, and clock frequencies and produce reproducible designs.

B. Technologies and Operating Points

We compare two CMOS technology nodes at a typical corner of 25 °C with different supply voltages V_{DD} and voltage threshold variants:

- **TSMC 16FFC FinFET CMOS 16 nm:**
  Standard-Voltage-Threshold SVT 0.80 V, 0.55 V
  Ultra-Low-Voltage-Threshold ULVT 0.80 V, 0.55 V
- **GlobalFoundries 22FDX FDSOI 22 nm:**
  Low-Voltage-Threshold LVT 0.80 V, 0.50 V
  Ultra-Low-Voltage-Threshold ULVT 0.80 V, 0.50 V

Same voltages are not enforced across all technologies due to technology-library availability; instead, comparable operating voltages are selected per library. For brevity, the two technologies are referred to as **16 nm** and **22 nm** respectively.

C. Sweep Experiment Design

For each node and operating point in Section III-B (8 in total) we sweep: all supported $d \in \{1, 2, 3, 4\}$, folding factors $L \in \{1, 2, 4, 8, 12, 16\}$, and a grid of clock frequencies $f_{\mathrm{CLK}} \in \{0.2, 0.4, 0.625, 1, 2, 5\}$ GHz. Points that violate

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

This document is a preprint of: D. Swist, S. Friedrich, E. Matus et al., "Power Profiling of a High-Throughput RLL Encoder for THz Communications," in Proceedings of 2026 International Conference on Mobile and Miniaturized Terahertz Systems (ICM2TS 2026), Skukuza, South Africa, Jul 2026.

timing constraints are recorded but excluded from energy comparisons. A total of 1152 configurations are evaluated.

The stimulus signals are random, independent and identically distributed input bits corresponding to the RLL encoder input bits carrying the information. A pass/fail flag is recorded for each run for functional verification. To ensure reproducibility, we retain the stimulus data and netlist activity VCD used for power analysis for each configuration (technology node, d, L, and frequency).

IV. Power Profiling Results

A. Power Statistics and Breakdown

Table II summarizes the power consumption and gives a breakdown for each technology and operating point, averaged over all timing-clean design configurations (all combinations of d, L, and f_{CLK}). The considered 22 nm technology nodes slightly outperform the 16 nm nodes on average in terms of power consumption. The breakdown reveals that switching power accounts for approximately 57% and internal power for 42% of the total (both dynamic power). Low-V_{DD} variants (i.e., $0.50\,\mathrm{V}$ and $0.55\,\mathrm{V}$) exhibit significantly lower overall power consumption compared to the high-V_{DD} ($0.80\,\mathrm{V}$) ones for all technology nodes, reflecting the power scaling with V_{DD} [7]. Leakage (static power) is higher on the ULVT variants compared to the SVT/LVT ones, as expected [8], [9], but remains negligible, contributing less than 1% on average at the typical-typical corner (TT/25 °C). The consistency of this breakdown across all configurations, with average deviations of $8.8\,\%$ for switching and $8.5\,\%$ for internal power from their respective averages, justifies focusing on total power in subsequent analyses, as the relative contributions remain nearly constant over the considered parameter space.

Among the technology variants, SVT and LVT options have a lower power consumption on average compared to the ULVT variants for a given V_{DD}, although they are of the same order of magnitude. Moreover, the low-V_{DD} configurations of those technology nodes exhibit the lowest average power among all configurations. However, the ULVT nodes have more relaxed timing constraints, which increases timing-clean parameter space. Consequently, subsequent detailed analysis focuses particularly on ULVT variants.

B. Clock-Frequency Sensitivity

The sensitivity of the power consumption and energy per bit to the clock frequency f_{CLK} is examined for the folding factor $L = 4$ as a representative example where enough configurations passed the timing check. Figures 3 and 4 reveal several key trends which are consistent across other folding factors, with the primary difference being the frequency range where timing constraints are met. Power scales approximately linearly with f_{CLK}, as expected from the CMOS power law [7], except for frequency regions approaching the timing constraint indicated by the right end of the individual curves. There, the synthesized netlist is more complex to meet timing constraints, leading to a superlinear increase in power, e.g., as visible for $d \in \{3, 4\}$. This effect is also visible in the energy-per-bit E_{b} evaluation in Fig. 4. E_{b} increases sharply close to the timing limit. Moreover, low-V_{DD} configurations (dashed lines) consistently operate at lower power compared to the high-V_{DD} ones for a given f_{CLK}, as explained above. However, timing limits are severely more restrictive at low voltages, leading to a narrower synthesizable frequency range as seen for most $d \in \{1, 2\}$. In conjunction with the more complex FSM codes $d \in \{3, 4\}$ as per Table I even the higher-voltage configurations fail timing constraints as seen in both Figures 3 and 4. Across technology families, 22 nm shows better performance than 16 nm in most cases as indicated by the average power consumption values.

TABLE II
Power Breakdown by Technology

Technology	P_{T} (mW)	Breakdown (%)			Range (mW)	
		Swt.	Int.	Leak.	Min	Max
22 nm LVT @ 0.80V	0.32	59.2	40.7	0.1	0.02	1.67
22 nm LVT @ 0.50V	0.04	61.9	37.6	0.0	0.01	0.10
22 nm ULVT @ 0.80V	0.44	56.8	41.6	1.7	0.02	3.17
22 nm ULVT @ 0.50V	0.09	57.9	39.9	2.1	0.01	0.30
16 nm SVT @ 0.80V	0.33	56.9	43.2	0.0	0.02	1.85
16 nm SVT @ 0.55V	0.07	60.1	39.9	0.0	0.01	0.39
16 nm ULVT @ 0.80V	0.65	53.6	45.5	0.9	0.03	5.08
16 nm ULVT @ 0.55V	0.19	55.0	43.5	1.4	0.01	1.15
All (avg)	0.32	57.0	42.1	0.9	0.02	2.09

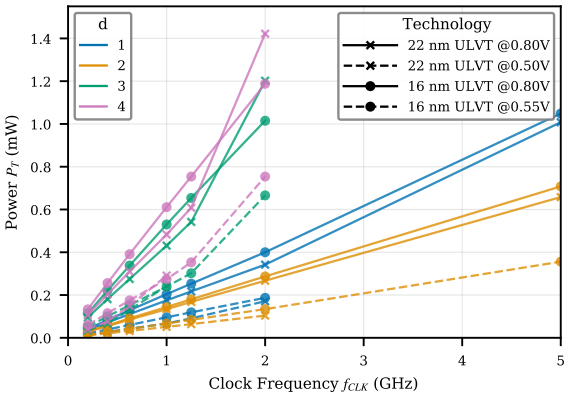

Fig. 3. Power versus clock frequency for folding factor $L = 4$ and all minimum runlength constraints d in Table I.

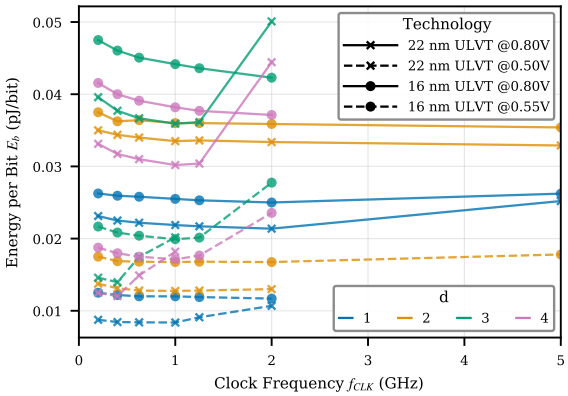

Fig. 4. Energy per bit versus clock frequency for folding factor $L = 4$ and all minimum runlength constraints d in Table I.

C. Folding Factor Impact

The power scaling with the folding factor L at $f_{\mathrm{CLK}} = 1.0\,\mathrm{GHz}$ is shown in Fig. 5, and the corresponding energy-

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

This document is a preprint of: D. Swist, S. Friedrich, E. Matus et al., "Power Profiling of a High-Throughput RLL Encoder for THz Communications," in Proceedings of 2026 International Conference on Mobile and Miniaturized Terahertz Systems (ICM2TS 2026), Skukuza, South Africa, Jul 2026.

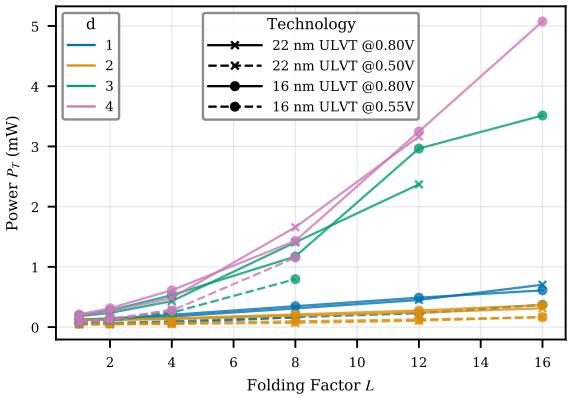

Fig. 5. Power versus folding factor L at 1.0 GHz and for all minimum runlength constraints d in Table I.

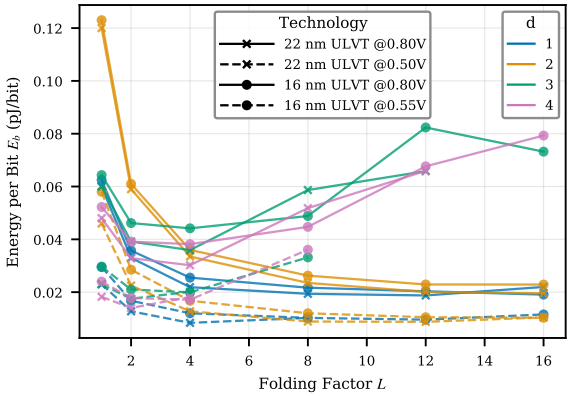

Fig. 6. Energy per bit versus folding factor L at 1.0 GHz and for all minimum runlength constraints d in Table I.

per-bit scaling is shown in Fig. 6. Timing constraints again significantly shape the achievable design space, with some high-L configurations failing timing constraints, particularly for low-voltage operating conditions and higher-complexity FSMs $d \in \{3, 4\}$. Fig. 5 shows a superlinear trend, and the energy-per-bit curves in Fig. 6 show broad minima. At low L, E_b is high and starts to decrease sharply with increasing L for every single configuration regardless of technology choice. This is because the increased logic datapath allows for more synthesis optimization options, while also the number of bits processed per clock cycle increases linearly with L. However, beyond certain L, the energy starts to rise again for $d \in \{3, 4\}$, since timing requirements severely increase necessary logic complexity. This is less apparent for $d \in \{1, 2\}$ within the shown L range, but a similar trend is expected for even higher L values, since the configurations are not yet at the timing limits w.r.t. L. Voltage scaling remains an effective optimization across all L and all nodes, and varying L is advantageous for optimizing energy efficiency.

D. Design-Space Energy Landscapes

The results in Sections IV-B and IV-C reveal clock-frequency- and folding-factor-dependent trends. To expose how these axes interact, we map E_b over the full two-dimensional parameter space of f_CLK and L. Fig. 7 shows the resulting energy landscapes focusing on the 22 nm nodes due to their lower average power consumption. The LVT and ULVT variants are shown at 0.80 V and 0.50 V for $d = 1$ (top row) and $d = 4$ (bottom row). Color encodes energy per bit at timing-clean points. Timing violations are displayed in a hatched, rose-colored pattern to delineate the feasible design region.

Energy valleys tend to occur close to the timing cliffs, i.e., regions where timing constraints are violated. This is consistent with Section IV-B where E_b starts to increase severely with f_CLK at the edge towards the timing limits. It is clearly visible that low L values lead to highly inefficient operation for all configurations. Moreover, from the heatmaps it is apparent that the low-V_DD configurations perform best in terms of energy efficiency. It is also visible that low-V_DD ULVT configurations allow optimization to the lowest possible E_b values within the design space. However, they do not outperform other configurations for every point in the design space. The energy per bit varies widely, with the ULVT variants having the lowest and highest values across the entire design space.

An advantage of the ULVT libraries is the larger timing margin, which is visible in their wider synthesizable parameter space. The timing constraints are most severe for complex FSMs (e.g., $d = 4$), where significantly more configurations pass the constraint check with the ULVT libraries compared to the LVT ones. In addition, the heatmaps show that the minimum E_b can be achieved by jointly tuning f_CLK and L to operate close to, but not at the timing cliffs. If high-speed operation demands a wider synthesizable region, V_DD can be increased at the cost of energy efficiency.

V. System-Level Operating Points

Based on the power profiling results, we identify best design configurations for achieving a target throughput of 100 Gbps. Individual encoders cannot reach such high throughputs alone due to timing constraints, and the limitations are even more severe for low-power configurations which favor reduced clock frequencies. To achieve such high throughput, we consider the parallel instantiation of P encoder units, each of which operates at a clock frequency of f_CLK and a folding factor of L, as proposed in [4]. Accordingly, block processing with padding of d zeros between the individual encoder lanes is considered to meet the minimum d constraint. To mitigate the code rate reduction from block processing, D consecutive output blocks of the individual encoders are concatenated before multiplexing the outputs of all parallel encoder blocks. This causes a net rate reduction from the nominal rate, leading to a system throughput of [4]:

$$T_\mathrm{S} = P \cdot T \cdot \frac{L \cdot D}{L \cdot D + d/q} = P \cdot T \cdot r \tag{1}$$

TABLE III
Best System-Level Parameters (all 22 nm, $D = 5$)

d	Technology	f_CLK (GHz)	L	P	T_S (Gbps)	P_S (mW)	$E_\mathrm{b,S}$ (fJ/bit)
1	ULVT @0.50V	0.200	16	16	102.0	0.736	7.2
2	LVT @0.50V	0.200	16	32	101.1	0.736	7.3
3	ULVT @0.50V	0.400	4	21	98.7	1.407	14.3
4	ULVT @0.50V	0.400	4	21	98.3	1.617	16.4

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

This document is a preprint of: D. Swist, S. Friedrich, E. Matus et al., “Power Profiling of a High-Throughput RLL Encoder for THz Communications,” in Proceedings of 2026 International Conference on Mobile and Miniaturized Terahertz Systems (ICM2TS 2026), Skukuza, South Africa, Jul 2026.

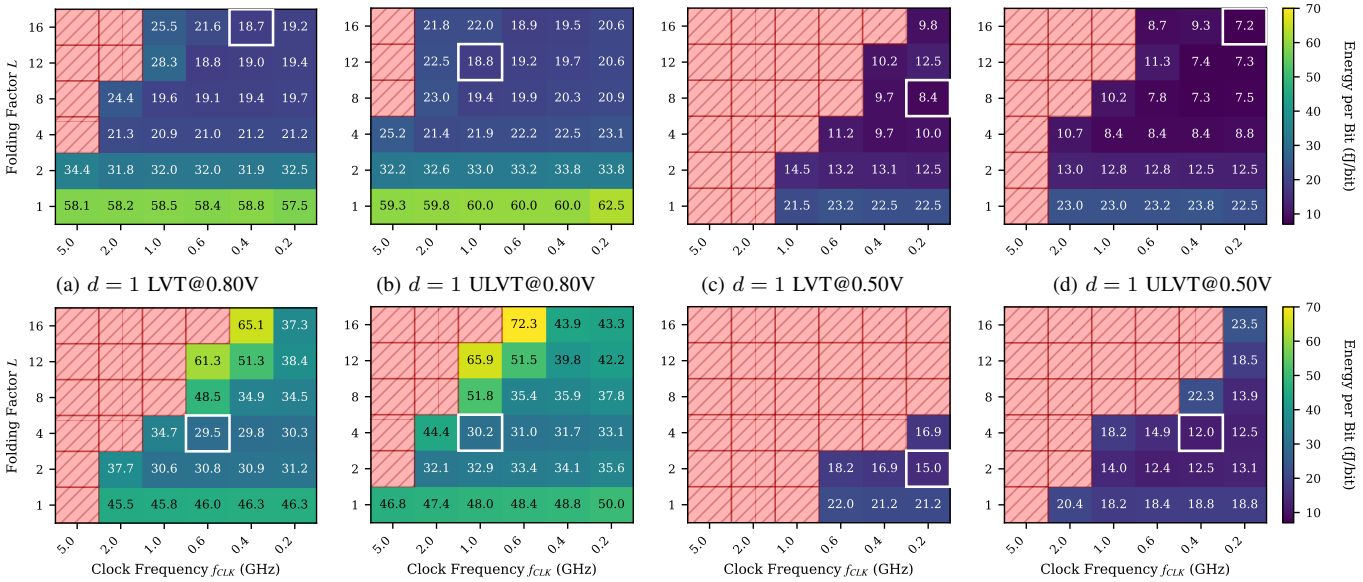

Fig. 7. Energy per bit E_b (pJ/bit) across f_CLK and L for all 22 nm technology configurations, shown for minimum runlength constraints $d = 1$ and $d = 4$ (Table I). Best value marked with white border.

with r being the reduction factor due to block processing. Likewise, the system-level energy per bit $E_{\mathrm{b,S}}$ is increased by the reciprocal of the reduction factor. Hence, the power consumed by the system is then $P_\mathrm{S} = P \cdot P_\mathrm{T}$, where other interface components are omitted for simplicity. Table III summarizes the best configurations to achieve a throughput of approximately 100 Gbps for each d among the entire considered design space along with their key performance metrics and the choice of $D = 5$. It is worth noting that the best configurations are all 22 nm technology nodes, which had the lowest V_DD libraries available for analysis. This also underlines the importance of the power scaling law [7]. The achieved energy per bit is below 0.020 pJ/bit for all d, which is significantly lower than the expected power for channel coding, e.g., by LDPC encoders. In this regard, for a rate of 257.9 Gbps in [10] a power consumption of 123.5 mW has been reported, resulting in 0.479 pJ/bit. Scaling the RLL encoder to a target of 1 Tbps could be achieved by increasing P by a factor of 10, and hence the power P_S as well. Looking at the absolute power values, this seems feasible within a power budget of a few Watts.

VI. Discussion and Conclusion

This work provides a comprehensive power profiling of a high-throughput RLL encoder design for THz ZXM systems, revealing that energy per bit can be minimized to a range between 7.2 fJ/bit and 16.4 fJ/bit. Cross-technology analysis shows that the considered 22 nm technology outperforms the 16 nm one in energy efficiency, with the ULVT variant performing best in most cases. As expected, voltage scaling has a huge impact, and low-voltage operating points provide the best performance. System-level projections indicate feasibility for 100 Gbps to 1 Tbps throughputs with parallel encoders. Investigating specialized ultra-low-power technology nodes alongside alternative RLL code structures could enable additional energy optimizations beyond current limits.

References

[1] B. Murmann, “ADC Performance Survey 1997-2025,” [Online]. Available: https://github.com/bmurmann/ADC-survey.

[2] P. Neuhaus, M. Dörpinghaus, and G. Fettweis, “Zero-crossing modulation for wideband systems employing 1-bit quantization and temporal oversampling: Transceiver design and performance evaluation,” *IEEE Open J. Commun. Soc.*, vol. 2, pp. 1915–1934, 2021.

[3] G. P. Fettweis, M. Dörpinghaus, S. Bender, L. T. N. Landau, P. Neuhaus, and M. Schlüter, “Zero crossing modulation for communication with temporally oversampled 1-bit quantization,” in *Proc. 53rd Asilomar Conf. Signals, Systems, and Computers*, Pacific Grove, CA, USA, Nov. 2019, pp. 207–214.

[4] D. Swist, S. Friedrich, E. Matúš, M. Dörpinghaus, and G. Fettweis, “Implementation aspects of RLL encoding for zero-crossing modulation based wideband communications,” in *Proc. 2025 Int. Conf. on Mobile and Miniaturized Terahertz Systems (ICMMTS)*, Dubai, UAE, Feb. 2025, pp. 1–5.

[5] G. P. Fettweis, M. Dörpinghaus, J. Castrillon, A. Kumar, C. Baier, K. Bock, F. Ellinger, A. Fery, F. H. P. Fitzek, H. Härtig, K. Jamshidi, T. Kissinger, W. Lehner, M. Mertig, W. E. Nagel, G. T. Nguyen, D. Plettemeier, M. Schröter, and T. Strufe, “Architecture and advanced electronics pathways toward highly adaptive energy-efficient computing,” *Proceedings of the IEEE*, vol. 107, no. 1, pp. 204–231, 2019.

[6] H. Zhang, D. Swist, A. B. Triantafyllos, M. Dörpinghaus, M. AlonsodelPino, G. Fettweis, and N. Llombart, “Towards energy-efficient high-speed THz communications links,” in *Proc. 28th European Microwave Week (EuMW)*, Utrecht, Netherlands, Sep. 2025, pp. 1–4.

[7] H. Veendrick, “Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits,” *IEEE Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, 1984.

[8] S. Borkar, “Design challenges of technology scaling,” *IEEE Micro*, vol. 19, no. 4, pp. 23–29, 1999.

[9] S. G. Narendra and A. Chandrakasan, *Leakage in Nanometer CMOS Technologies*, ser. Integrated Circuits and Systems. New York, NY: Springer, 2006.

[10] Y. Tian *et al.*, “Low-latency QC-LDPC encoder design for 5g NR,” *Sensors*, vol. 21, no. 18, p. 6266, Sep. 2021.

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.