PSO-based Output Matching Network for Concurrent Dual-Band LNA

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***Abstract*—This article presents an original design methodology for the selection of output matching load network for a dual-band Low Noise Amplifier (LNA) that is targeted for the use in the GSM 1.8 GHz and WLAN 2.4 GHz range. A particle swarm optimization (PSO) based technique is used to get the optimized values of the output load network components. The concurrent dual-band LNA is simulated with these entire component values in CADENCE with CMOS 0.18µm technology.**

***Index Terms*—Dual-band concurrent Low Noise Amplifier, Output Matching Network, Particle Swarm Optimization based technique.**

I. Introduction

MULTISTANDARD wireless communication systems are becoming popular day by day and this makes the combination of two or more radio-frequency (RF) bands in one wireless receiver desirable. In these dual-band wireless receivers, dual-band low-noise amplifiers (LNAs) are one of the main component blocks. Designed to have low-noise figures, the LNAs also increase the sensitivity of the dual-band wireless receivers and also have high linearity to prevent interference from undesired signals.

There are several implementations covering GSM or WLAN b/g/a frequencies. But they use parallel LNAs which is not a cost efficient solution. A concurrent LNA is therefore a better choice because it enables saving die area and power consumption when compared to the parallel LNA approach.

A few CMOS concurrent implementations have already been proposed [1], [2]. However, there is no information about the selection of dual-band input/output network elements. In this article we explore the concurrent LNA topology using 0.18 µm CMOS9 process.

This article is organized as follows. In section II, we describe the general concurrent LNA design theory. There we discuss about the input matching theory and also discuss about the switching topology which matches the dual-band LNA to either selection procedure for the output network elements.

In section III, we provide a detailed description of an original synthesis method. This procedure aids in selecting the values for the concurrent output matching network element.

In section IV, we apply this methodology to design a concurrent dual-band LNA dedicated to work in GSM 1.8 GHz and WLAN 2.4 GHz range.

II. LNA Design Methodology

A. Description of LNA Topology

Fig. 1 shows the proposed LNA. It adopts a cascode structure which has a lot of advantages such as an excellent input/output isolation, high gain, and reduced Miller effect.

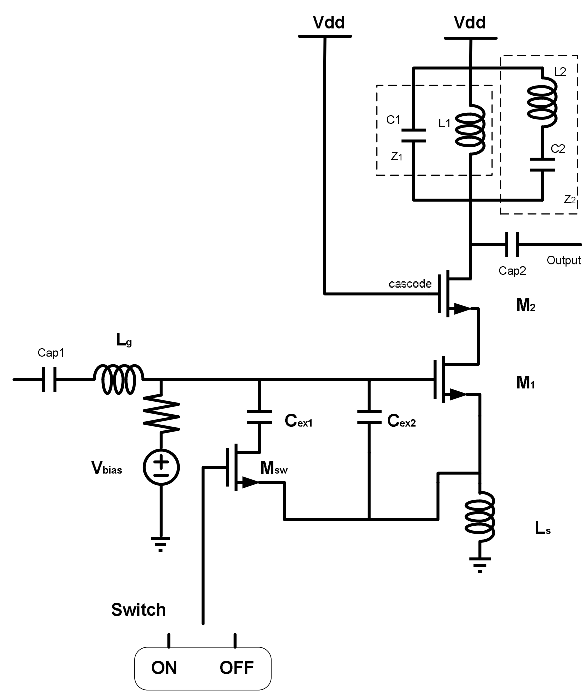

Fig. 1. Schematic of the proposed dual-band LNA

NMOS switches are used, whose performance degradations are minimized by employing the parallel connection. The size of the switch is determined by considering the on-resistance and capacitance of it. The LNA uses the same input/output matching components for both frequencies except the switch controlled C_{ex1}.

B. Input Matching Theory

The resistance of the matching circuit is assumed small. As the switch is turned on for the 1.8 GHz, the input impedance of the LNA is given by

$$Z_{in_1} = j(\omega_1 L_g + \omega_1 L_s - \frac{1}{\omega_1 (C_{gs} + C_{ex1} + C_{ex2})}) + \frac{g_m L_s}{(C_{gs} + C_{ex1} + C_{ex2})} \quad (1)$$

Where g_m , C_{gs} and ω_1 are the transconductance , the gate-source capacitance, and the operating frequency respectively. For optimal matching the following condition is to be satisfied

$$Z_{opt} = Z_{in}^{*} = Z_s \quad (2)$$

To satisfy the optimum matching conditions in (2), the L_g , L_s and W/L should be selected properly with an appropriate bias condition. The L_s should be optimized appropriately as it enables simultaneous impedance and noise matching without any significant degradation of Noise Figure.

For the 2.4 GHz operation, the switch is turned off, and the input impedance is given by

$$Z_{in_2} = j(\omega_2 L_g + \omega_2 L_s - \frac{1}{\omega_2 (C_{gs} + C_{ex2})}) + \frac{g_m L_s}{(C_{gs} + C_{ex2})} \quad (3)$$

As evident from (1) and (3) the input impedance at 2.4 GHz is changed by the switch. Just by switching the external capacitor C_{ex1} on, simultaneous noise and input matching at 1.8 GHz are achieved.

III. Output Matching Theory

A. Output Matching with ideal elements

An analysis is carried out to help select the output network element values.

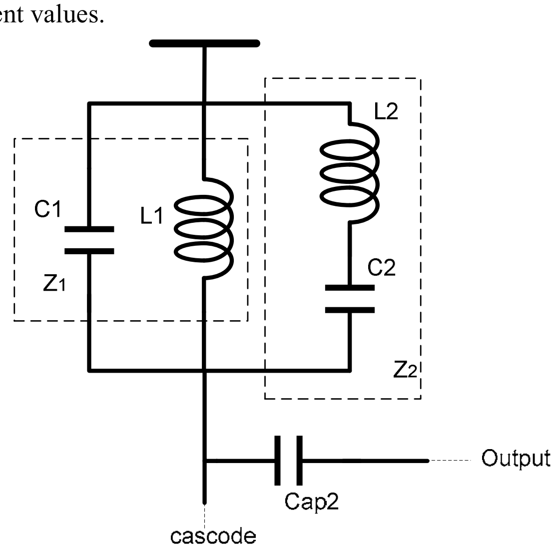

Fig. 2. Concurrent output matching network (simplified).

Neglecting the effect of output series capacitance 'Cap2', the analysis of the mutual resonance condition of output concurrent load is simplified. The expression of the resulting impedance is

$$Z = \frac{sL_1(1+s^2L_2C_2)}{1+s^2(L_1C_1+L_2C_2+L_1C_2)+s^4L_1C_1L_2C_2} \quad (4)$$

From the above expression, the characteristic equation involving frequency ω, is:

$$1-\omega^2(L_1C_1+L_2C_2+L_1C_2)+\omega^4L_1C_1L_2C_2 = 0 \quad (5)$$

The roots of the above equation (2) are given by the following expression.

$$\omega_{1,2} = \sqrt{\frac{\frac{C_1}{C_2}+\frac{L_2}{L_1}+1 \pm \sqrt{(\frac{C_1}{C_2}+\frac{L_2}{L_1}+1)^2 - 4\frac{C_1L_2}{C_2L_1}}}{2C_1L_2}} \quad (6)$$

The design procedure followed is described briefly in the following few lines. The input parameters of this design are the two resonant frequencies ω_1, ω_2 and the series capacitance C_2 from (4). On the basis of (5) we define two variables S and P:

$$S = \omega_1^2 + \omega_2^2 = \frac{L_1C_1+L_2C_2+L_1C_2}{L_1C_1L_2C_2} \quad (7)$$

And

$$P = \omega_1^2\omega_2^2 = \frac{1}{L_1C_1L_2C_2} \quad (8)$$

The main aim is to design an appropriate notch frequency around ω_1 and ω_2 and also obtain low inductance values for L_1 and L_2. For this we select the notch frequency to be

$$\omega_0 = \frac{\omega_1+\omega_2}{2} \quad (9)$$

Now with the knowledge of the values of C_2 and ω_0 where $\omega_0 = \frac{1}{\sqrt{L_2C_2}}$, we can find out L_2. Now the value of L_1C_1 is found out from the equation

$$\frac{1}{L_1C_1} = \frac{P}{\omega_0^2} \quad (10)$$

And writing (4) as

$$S = \frac{1}{L_2C_2}+\frac{1}{L_1C_1}+\frac{1}{L_2C_1} \quad (11)$$

We find out the numerical value of $\frac{1}{L_2C_1}$. Now with the knowledge of L_2 we find out C_1 and then from (10) we calculate L_1.

TABLE I
Component Values

C_2 (pF)	L_2 (nH)	C_1 (pF)	L_1 (nH)
0.41	14.00	5.00	1.20
0.60	9.58	7.40	0.81
1.00	5.75	12.33	0.49
2.00	2.87	24.67	0.24

Table I gives the component values of the output network. These values are obtained considering ideal components. Hence significant shift is noticed in theoretical and simulation values when these component values are used in the output network circuit. Considering non-ideal components, the design is modified and is described in the next section

B. Design of Output Network with non-ideal components

Non-ideal inductors having a quality factor Q_L modify the expression of the impedance of the output load network as shown:

$$Z=\frac{sL_1(1+s^2L_2C_2(1-\frac{j}{Q_L}))(1-\frac{j}{Q_L})}{1+s^2(L_1C_1+L_2C_2+L_1C_2)(1-\frac{j}{Q_L})+s^4L_1C_1L_2C_2(1-\frac{j}{Q_L})^2} \quad (12)$$

Arranging the numerator and denominator of the above expression in real and imaginary form, we get

$$Z=\frac{sL_1(1+s^2L_2C_2(1-\frac{1}{Q_L^2}))-\frac{j}{Q_L}sL_1(1+2s^2L_2C_2)}{1+s^2(L_1C_1+L_2C_2+L_1C_2)+s^4L_1C_1L_2C_2(1-\frac{1}{Q_L^2})-\frac{j}{Q_L}(s^2(L_1C_1+L_2C_2+L_1C_2)+2s^4L_1C_1L_2C_2)} \quad (13)$$

Equation (13) can be rewritten as

$$Z=\frac{a-jb}{c-jd}=\frac{(ac-bd)}{c^2+d^2}-j\frac{(bc-ad)}{c^2+d^2} \quad (14)$$

Where a and b are real and imaginary part of numerator, c and d are the real and imaginary part of the denominator of (13). Making the imaginary part of output impedance zero, we get the following equation.

$$\omega^4(1+\frac{1}{Q_L^2})(L_2^2C_2^2+L_1C_2^2L_2)-2L_2C_2\omega^2+1=0 \quad (15)$$

From the above equation, the roots of the equation, which are also the matching frequencies, are:

$$\omega_{1,2}=\sqrt{\frac{2L_2C_2\pm\sqrt{(2L_2C_2)^2-4(1+\frac{1}{Q_L^2})(L_2^2C_2^2+L_1C_2^2L_2)}}{2(1+\frac{1}{Q_L^2})(L_2^2C_2^2+L_1C_2^2L_2)}} \quad (16)$$

The design procedure followed is described briefly in the following few lines. The input parameters of this design are the two resonant frequencies ω_1, ω_2 and the series capacitance C_2 from equation. On the basis of (15) we define two variables S_1 and P_1:

$$S_1=\omega_1^2+\omega_2^2=\frac{2L_2C_2}{(1+\frac{1}{Q_L^2})(L_2^2C_2^2+L_1C_2^2L_2)} \quad (17)$$

And

$$P_1=\omega_1^2\omega_2^2=\frac{1}{(1+\frac{1}{Q_L^2})(L_2^2C_2^2+L_1C_2^2L_2)} \quad (18)$$

The notch frequency is selected as before;

$$\omega_0=\frac{\omega_1+\omega_2}{2} \quad (19)$$

Now with the values of C_2, ω_1 and ω_2 we calculate S_1 and P_1. Now from (17) and (18) we have

$$L_2=\frac{1}{2C_2}(\frac{S_1}{P_1}) \quad (20)$$

Now knowing the quality factor Q_L , the value of L_1 is found out from (17). Now making the real part of the expression in (14) equal to 50 ohms, we calculate the value of C_1.

C. PSO based technique for synthesis of output network

Several heuristic algorithms like Genetic Algorithm (GA), simulated annealing, particle swarm optimization (PSO) etc. are used in finding optimal design solutions of RF – analog circuits. The PSO is an agent based stochastic evolutionary computation technique, based on the movement and intelligence of swarms. Difficult multi dimensional problems have been effectively optimized by the PSO based technique [3].

The PSO tries to reach at an optimum solution by modifying the velocity of each particle depending on the best solutions achieved by the individual particles:

$$v_{new}=v_{old}+k_1p_1(best_{personal}-present)+k_2p_2(best_{global}-present) \quad (21)$$

The new position of the particle is defined by the following equation:

$$present=present+v_{new} \quad (22)$$

In the above equations, p_1, p_2, k_1 and k_2 are constants which are to be appropriately chosen for convergence of the solution towards the global optimum.

In this paper, the PSO technique is efficiently applied to the problem of finding the component values of the output matching network of the dual-band LNA at a specified carrier frequency, over a given bandwidth. Table II lists the component values obtained considering finite Q_L and using the PSO based optimization technique.

TABLE II
COMPONENT VALUES OF OUTPUT MATCHING NETWORK

Non Ideal Component Values				PSO based Component Values			
C_2 (pF)	L_2 (nH)	C_1 (pF)	L_1 (nH)	C_2 (pF)	L_2 (nH)	C_1 (pF)	L_1 (nH)
0.40	15.20	5.30	1.50	0.84	15.00	10.00	2.10
0.60	10.18	7.60	1.16	0.50	12.00	6.00	1.00
1.00	8.30	12.67	0.70	0.40	10.00	5.10	0.70
2.00	6.60	25.67	0.35	0.38	8.00	4.50	0.50

IV. LNA DESIGN EXAMPLE AND SIMULATION RESULTS

In this section we demonstrate the design of a dual-band concurrent LNA operating at GSM 1.8 GHz and WLAN 2.4 GHz using CMOS 0.18 µm technology. Based on the Output Matching theory outlined in Section III, a PSO based optimization technique is used to obtain the component values of the tank load network. From the table of inductor and capacitor values obtained using the PSO based algorithm (Table II), L_1=1 nH, C_1=6 pF, L_2=12 nH, C_2=0.5 pF have been chosen for a practical design implementation. Fig.3 shows the real component of the output impedance of the proposed topology. The real part of the output impedance is 42 Ω at 1.8 GHz and 51 Ω at 2.4 GHz matching closely with the expected value. The imaginary component of the output impedance is -3.5 Ω at 1.8 GHz and -7Ω at 2.4 GHz deviating from the expected zero value due to device capacitances.

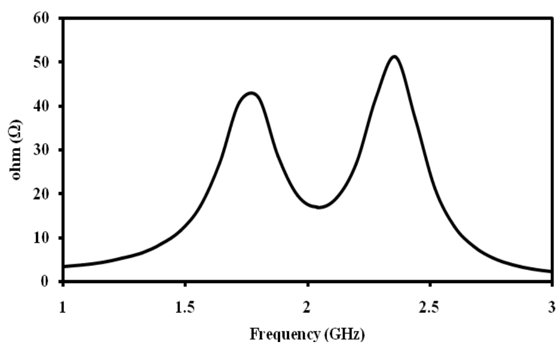

Fig. 3. Real part of output impedance.

The effect of the input matching network is shown in Fig.4 while Fig.5 highlights the voltage gain and the output matching obtained using the concurrent topology. The concurrent dual-band LNA demonstrates a voltage gain of 9 dB at 1.8 GHz and 7.8 dB at 2.4 GHz with an output matching of -20 dB in both bands of operation. The NF of the circuit is 2.1 dB at 1.8 GHz and 2.4 dB at 2.4 GHz for a total drain current of 10 mA with 1.8 V power supply. A high drain current of 10 mA is required for GSM 1800 and WLAN 2.4 GHz frequency bands as the notch frequency lies very close to the bands of operation requiring inductors of high quality factor for good performance at low power. The present design uses inductors of Q=7.5 as available in CMOS 0.18 µm technology. Significant improvement in performance is expected if the design is implemented using RF substrates.

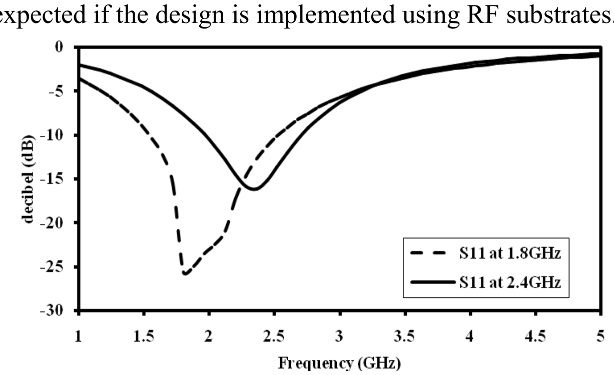

Fig. 4. Input Matching in concurrent dual band LNA

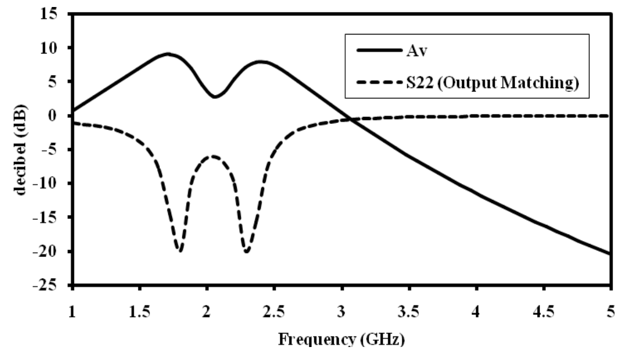

Fig. 5. Voltage Gain and Output Matching in concurrent dual band LNA

Table III summarizes the performance of the current design.

TABLE III
PERFORMANCE SUMMARY OF THE CONCURRENT DUAL BAND CMOS LNA

Frequency	1.8GHz	2.4GHz
Voltage Gain	9 dB	7.8 dB
S_{11}	-25.6 dB	-15.3 dB
S_{22}	-20 dB	-20 dB
NF	2.1 dB	2.4 dB
Input IP3	-2.53 dBm	-2.32 dBm
DC Current	10mA	
Supply Voltage	1.8V	

V. CONCLUSION

A design methodology for the selection of output matching network for concurrent dual band LNA has been proposed in this paper. A particle swarm based optimization technique has been used to obtain optimized component values of the output matching network incorporating the finite Q values of the components. A concurrent dual band LNA design example has been implemented using the output matching network obtained using the proposed technique while switched capacitors are used for input matching. The concurrent dual band LNA has been designed using CMOS 0.18 µm technology to operate in the 1.8 GHz GSM and WLAN 2.4 GHz frequency bands.

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REFERENCES

[1] Hossein Hashemi, Ali Hajimiri, "Concurrent Multiband Low-Noise Amplifiers—Theory, Design,and Applications" in *IEEE Trans. Microwave Theory Tech.*, , vol. MTT-50, pp. 288–301,Jan 2002.

[2] Ouail El-Gharniti, Eric Kerherve, Jean-Baptiste Begueret, Didier Belot, "Concurrent Dual-Band Low Noise Amplifier for 802.11a/g WLAN applications" in *IEEE International Conference on Electronics, Circuits and Systems*, Dec 2006, pp. 66-69.

[3] Ashudeb Dutta, Kaushik Dasgupta, T.K. Bhattacharyya, "Compact small signal modeling and PSO-based input matching of a packaged CMOS LNA in subthreshold region" in *Elsevier Microelectronics Journal* ,vol.38 , pp. 1050–1056, Sept 2007.