TECHNISCHE UNIVERSITÄT DRESDEN

Collaborative Research Center 912 – HAEC
Highly Adaptive Energy-Efficient Computing

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Motivation:

In 2012, information and communication technology already accounted for almost 5% of the worldwide electricity consumption with annual growth rates of 7% corresponding to a doubling per decade. To break this trend, it is important to enable highly energy-efficient computing infrastructures without compromising performance. This goal directly reflects the research vision addressed by the Collaborative Research Center HAEC (Highly Adaptive Energy-efficient Computing). To turn this vision into reality, HAEC addresses key research questions concerning hardware, software as well as system challenges by creating innovative leading edge technology for novel computing architectures and energy-adaptive hardware and software.

Objective:

HAEC aims for a holistic approach of energy adaptivity, taking into account energy efficiency at all levels as a joint optimization problem, ranging from the transistors, over the communication architecture up to the software engineering with an energy-aware computing management.

In the long term, HAEC strives to implement the vision of a HAEC Box, a highly performant but energy-adaptive computing platform with an overall volume of just one liter hosting 100 million of individual cores with TBytes of main memory. By utilizing novel chip integrated optical and flexible wireless chip-to-chip communication technology developed within HAEC, the HAEC Box will allow for a new level of run-time adaptivity of future computers. This enables a platform that flexibly adapts to the needs of different algorithmic problems. The HAEC Box employs multiple energy-control loops that adapt hardware and software components to achieve the best energy-performance trade-off for the current performance demand and workload type at run-time. Envisioning the one liter concept allows us to bring such servers closer to the user, e.g., by combining them with a WiFi router or cellular network base station, thus reducing net-work traffic and energy consumption of the global computing infrastructure significantly. To illustrate the potential of such a computing device, HAEC plans to have four printed circuit boards (PCB) with 16 compute nodes each connected via optical links on board and short-range wireless mm-wave links bet-ween compute nodes located at different PCBs.

It is planned that each compute node will have 128 layers (following an extremely ambitious 3D-stacking approach) with 1 million cores and 0.5 MByte main memory per core. As a result, the HAEC Box is expected to have 10^4 times the computing performance per unit volume compared to today's servers.

Approach:

To tackle the challenging research objective of HAEC, research projects are coordinated into three groups as the following:

The goal of the **HAEC-Hardware group** is to provide low-energy and highly adaptive interconnection technology based on optical and wireless links, including the development of packaging technology for the different process technologies required.

The goal of the **HAEC-Architecture group** is to provide a communication network based on the heterogeneous communication structure. Thereby, HAEC-Architecture is closely following the communication demands of the software structure using optimized network coding and routing taking energy efficiency into account. Also, security and delay constraints are of major importance to fulfill the requirements of the applications running on this new computer architecture.

The goal of the **HAEC-Software group** is to provide a comprehensive, energy-aware software infrastructure to make use of the versatile computing and network architecture provided by the HAEC-Hardware and the HAEC-Architecture group to enable a novel class of scalable and adaptive applications.